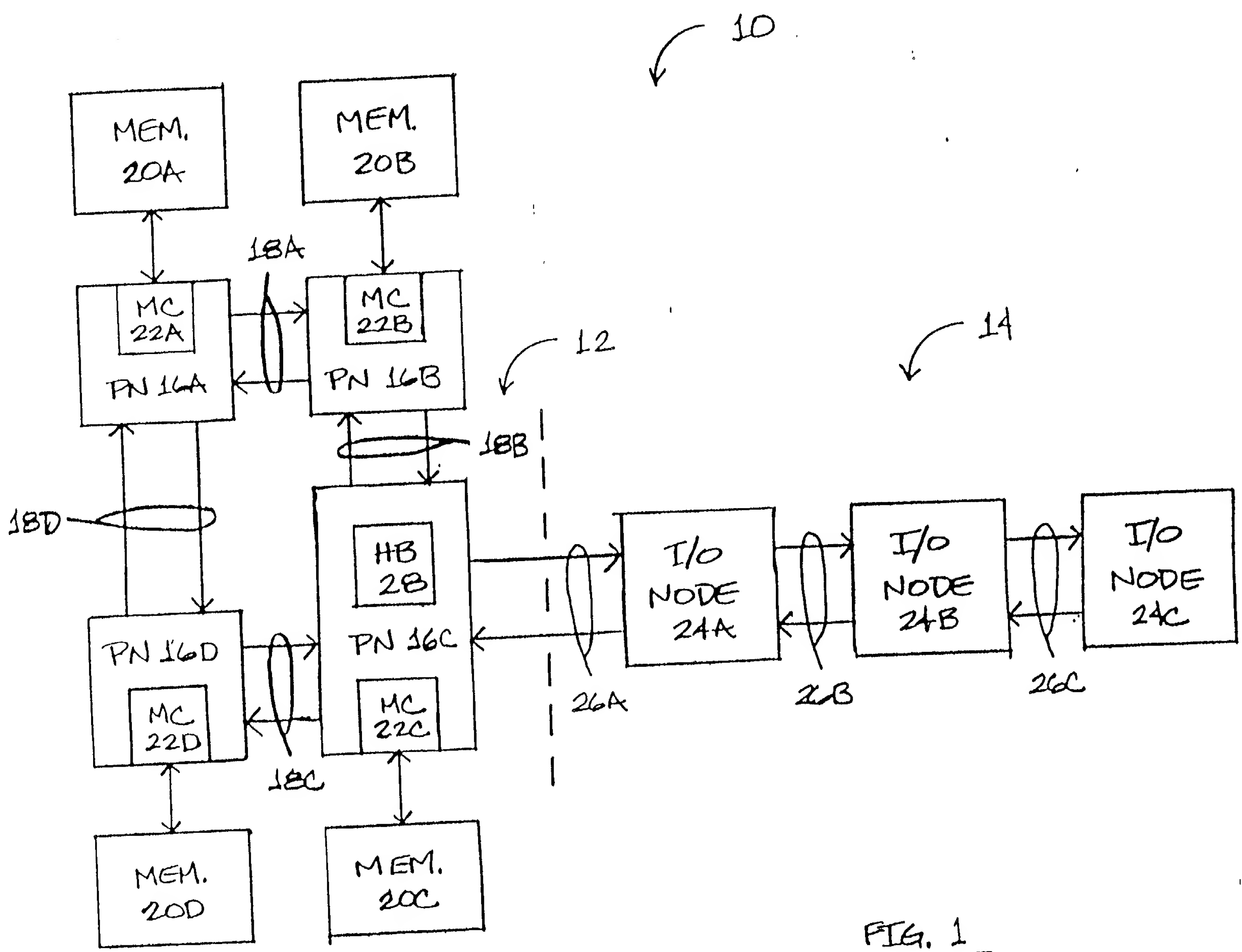
10
MEM. 20A
MEM. 20B
MC 22A
PN 16A
MC 22B
PN 16B
18A
12
14
18B
18D
HB 28
PN 16C
MC 22C
PN 16D
MC 22D
18C
I/O NODE 24A
I/O NODE 24B
I/O NODE 24C
26A
26B
26C
MEM. 20D
MEM. 20C

FIG. 1

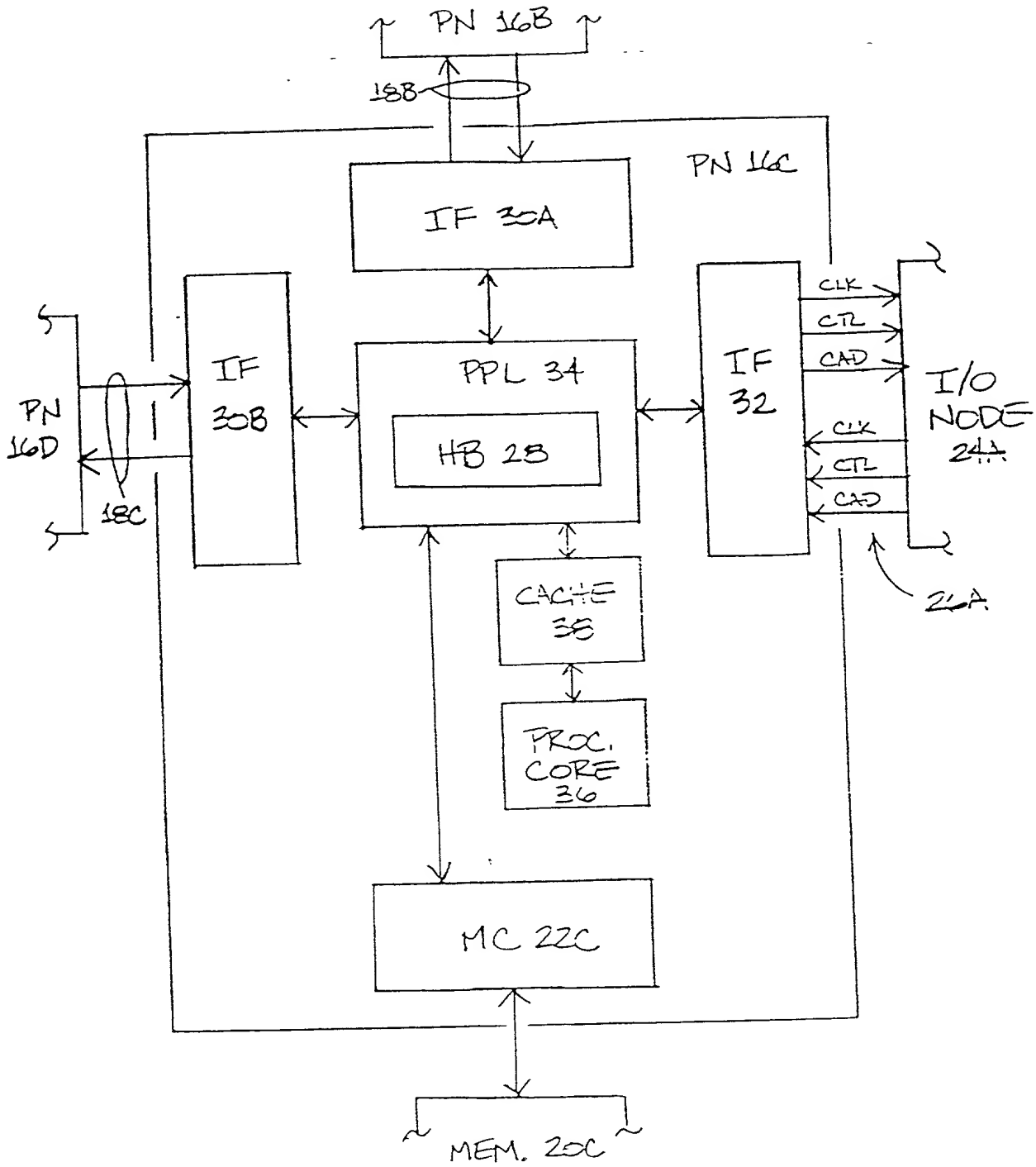
PN 16B
18B
PN 16C
IF 30A
IF 30B
PPL 34
HB 28
IF 32
CLK
CTL
CAD
I/O NODE 24A
PN 16D
18C
CLK
CTL
CAD
24A
CACHE 38
PROC. CORE 36
MC 22C
MEM. 20C

FIG. 2

Bit Time	7	6	5	4	3	2	1	0
0			CMD[5:0]					
1								
2								
3								

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FIG. 3

Bit Time	7	6	5	4	3	2	1	0
0	Src Unit [1:0]		CMD[5:0]					
1	DestNode[2:0]			Dest Unit[1:0]		SrcNode[2:0]		
2				SrcTag[4:0]				
3								
4	Addr[15:8]							
5	Addr[23:16]							
6	Addr[31:24]							
7	Addr[39:32]							

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FIG. 4

Bit Time	7	6	5	4	3	2	1	0
0	Src Unit [1:0]		CMD[5:0]					
1	DestNode[2:0]			Dest Unit[1:0]		SrcNode[2:0]		
2				SrcTag[4:0]				
3								

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FIG. 5

Bit Time	7	6	5	4	3	2	1	0
0	Data[7:0]							
1	Data[15:8]							
2	Data[23:16]							
3	Data[31:24]							
4	Data[39:32]							
5	Data[47:40]							
6	Data[55:48]							
7	Data[63:56]							

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FIG. 6

CMD Code	VChan	Command	Packet Type
000000	–	Nop	Info
000001	NPR	VicBlk	Request / Address / Data
000010	–	Reserved	–
000011	NPR	ValidateBlk	Request / Address
000100	NPR	RdBlk	Request / Address
000101	NPR	RdBlkS	Request / Address
000110	NPR	RdBlkMod	Request / Address
000111	NPR	ChangeToDirty	Request / Address
x01xxx	NPR or PR	Wr(Sized)	Request / Address / Data
01xxxx	NPR	Read(Sized)	Request / Address
100xxx	–	Reserved	–
110000	R	RdResponse	Response / Data
110001	R	ProbeResp	Response
110010	R	TgtStart	Response
110011	R	TgtDone	Response
110100	R	SrcDone	Response
110101	R	MemCancel	Response
11011x	–	Reserved	–
11100x	P	Probe	Request / Address
11101x	P	Broadcast	Request / Address
11110x	–	Reserved	–
111110	–	Reserved	–
111111	–	Sync	Info

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FIG. 7

Bit Time	7	6	5	4	3	2	1	0
0	SeqID[3:2]		CMD[5:0]					
1	Pass PW	SeqID[1:0]	UnitID[4:0]					
2			SrcTag[4:0]					
3	Addr[7:2]							
4	Addr[15:8]							
5	Addr[23:16]							
6	Addr[31:24]							
7	Addr[39:32]							

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FIG. 8

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Bit Time	7	6	5	4	3	2	1	0
0			CMD[5:0]					
1	Pass PW	Bridge		UnitID[4:0]				
2			Error	SrcTag[4:0]				
3			NXA					

FIG. 9

CMD Code	VChan	Command	Packet Type
000000	–	Nop	Info
000001	–	Reserved	–
000010	NPR	Flush	Request
000011	–	Reserved	–
0001xx	–	Reserved	–
x01xxx	NPR or PR	Wr(Sized)	Request / Address / Data
01xxxx	NPR	Read(Sized)	Request / Address
100xxx	–	Reserved	–
110000	R	RdResponse	Response / Data
110001	–	Reserved	–
110010	–	Reserved	–
110011	R	TgtDone	Response
11010x	–	Reserved	–
11011x	–	Reserved	–
11100x	–	Reserved	–
11101x	PR or NPR	Broadcast	Request / Address
111100	PR	Fence	Request
111101	–	Reserved	–
111110	–	Reserved	–
111111	–	Sync	Info

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Fig. 10

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FIG. 11

Request$_1$ TYPE	Request$_2$ TYPE	WAIT REQUIREMENTS
MEMORY WRITE	MEMORY WRITE	1. Req$_2$ MUST WAIT FOR TgtStart$_1$. 2. SrcDone$_2$ MUST WAIT FOR TgtDone$_1$. 3. TgtDone$_2$ ON THE NON-COHERENT LINK (IF REQUIRED) MUST WAIT FOR TgtDone$_1$.
MEMORY WRITE	MEMORY READ	1. Req$_2$ MUST WAIT FOR TgtStart$_1$. 2. TgtDone$_2$ ON THE NON-COHERENT LINK MUST WAIT FOR TgtDone$_1$.
MEMORY READ	MEMORY REQUEST	Req$_2$ MUST WAIT FOR TgtStart$_1$.
MEMORY WRITE	I/O REQUEST OR INTERRUPT	Req$_2$ MUST WAIT FOR TgtStart$_1$.
MEMORY READ	I/O REQUEST	Req$_2$ MUST WAIT FOR TgtStart$_1$.
MEMORY WRITE	FLUSH	TgtDone$_2$ ON THE NON-COHERENT LINK MUST WAIT FOR TgtDone$_1$. (FLUSH DOES NOT CAUSE ANY REQUESTS TO BE ISSUED TO THE COHERENT FABRIC.)
MEMORY READ	FLUSH OR INTERRUPT	NO WAIT REQUIREMENTS
MEMORY WRITE	RESPONSE	Response$_2$ MUST WAIT FOR TgtDone$_1$.
MEMORY READ	RESPONSE	Response$_2$ MUST WAIT FOR TgtStart$_1$.
I/O REQUEST	MEMORY REQUEST	Req$_2$ MUST WAIT FOR TgtStart$_1$.
I/O REQUEST	I/O REQUEST OR INTERRUPT	Req$_2$ MUST WAIT FOR TgtStart$_1$.
I/O REQUEST	FLUSH	TgtDone$_2$ ON THE NON-COHERENT LINK MUST WAIT FOR TgtStart$_1$. (FLUSH DOES NOT CAUSE ANY REQUESTS TO BE ISSUED TO THE COHERENT FABRIC.)
I/O REQUEST	RESPONSE	Response$_2$ MUST WAIT FOR TgtStart$_1$.
FLUSH	ANYTHING	NO WAIT REQUIREMENTS
RESPONSE	ANYTHING	NO WAIT REQUIREMENTS
FIXED / NON VECTORED INTERRUPT	RESPONSE	Response$_2$ MUST WAIT FOR ALL BROADCAST MESSAGE RESPONSES TO BE RECEIVED.
FIXED / NON VECTORED INTERRUPT	ANYTHING BUT RESPONSE	NO WAIT REQUIREMENTS
LPA INTERRUPT	ANYTHING	NO WAIT REQUIREMENTS
SysMgt	ANYTHING	NO WAIT REQUIREMENTS
FENCE	POSTED REQUEST	Req$_2$ MUST WAIT FOR FENCE TO BE RETIRED.
FENCE	ANYTHING NONPOSTED	NO WAIT REQUIREMENTS
POSTED MEMORY WRITE	FENCE	Req$_2$ MAY BE RETIRED WHEN TgtDone$_1$.
POSTED I/O WRITE	FENCE	Req$_2$ MAY BE RETIRED WHEN TgtStart$_1$.
ANYTHING NONPOSTED	FENCE	NO WAIT REQUIREMENTS

Bit Time	7	6	5	4	3	2	1	0
0	SrcUnit[1:0]		Cmd[5:0]					
1	TgtNode[2:0]			TgtUnit[1:0]		SrcNode[2:0]		
2	MD	Rsv		SrcTag[4:0]				
3	Addr[7:3]					NextState[1:0]		RD
4	Addr[15:8]							
5	Addr[23:16]							
6	Addr[31:24]							
7	Addr[39:32]							

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FIG. 12

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NextState[1:0]	Next State
0	No Change
1	Shared : Clean-> Shared Dirty->Shared/Dirty
2	Invalid
3	Rsv

FIG. 13

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Transaction Class	Probe Request	Next State	Memory Data	Return Data	Probe Response Tgt
RdSized (no lock, or locked by different requester)	Probe/Src	No change	1	1	SrcNode/SrcUnit
RdSized (locked by requester)	Probe/Src	Shared	1	1	SrcNode/SrcUnit
RdBlk, RdBlkS	Probe/Src	Shared	1	1	SrcNode/SrcUnit
RdBlkMod	Probe/Src	Invalid	1	1	SrcNode/SrcUnit
ChangeToDirty	Probe/Src	Invalid	0	1	SrcNode/SrcUnit
ValidateBlk	Probe/Src	Invalid	0	0	SrcNode/SrcUnit
WrSized	Probe/Tgt	Invalid	0	1 (0 is optional for 16 doubleword writes)	TgtNode/TgtUnit
VicBlk	No Probes Sent	-	-	-	-

FIG. 14

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Bit Time	7	6	5	4	3	2	1	0
0	SrcUnit[1:0]		Cmd[5:0]					
1	DestNode[2:0]			DestUnit[1:0]		SrcNode[2:0]		
2	Rsv		Error	SrcTag[4:0]				
3	Shared	Rsv						

FIG. 15

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Bit Time	7	6	5	4	3	2	1	0
0	SrcUnit[1:0]		Cmd[5:0]					
1	DestNode[2:0]			DestUnit[1:0]		SrcNode[2:0]		
2	Count[1:0]		Error	SrcTag[4:0]				
3	Shared	Probe	Rsv			Cancel	Count[3:2]	

FIG. 16

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Bit Time	7	6	5	4	3	2	1	0
0	SrcUnit[1:0]		Cmd[5:0]					
1	DestNode[2:0]			DestUnit[1:0]		SrcNode[2:0]		
2	Rsv		Error	SrcTag[4:0]				
3	Rsv					Cancel/ Rsv	Rsv	

FIG. 17

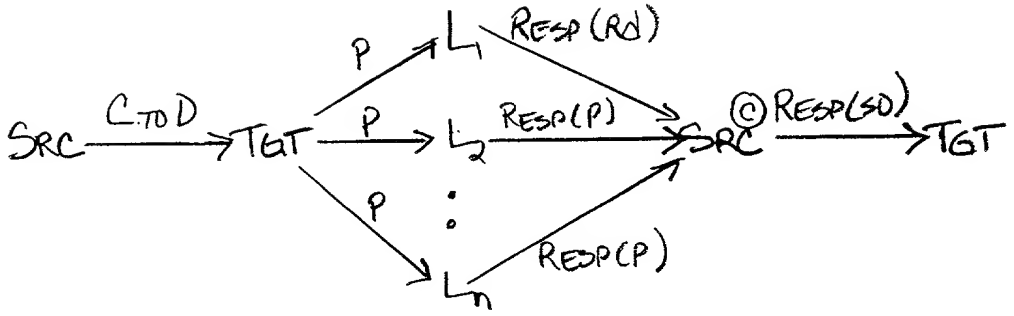
SRC
C.TO D
TGT
P
P
P
L1
L2
Ln
RESP (Rd)
RESP(P)
RESP(P)
©
RESP(SD)
SRC
TGT

FIG. 23

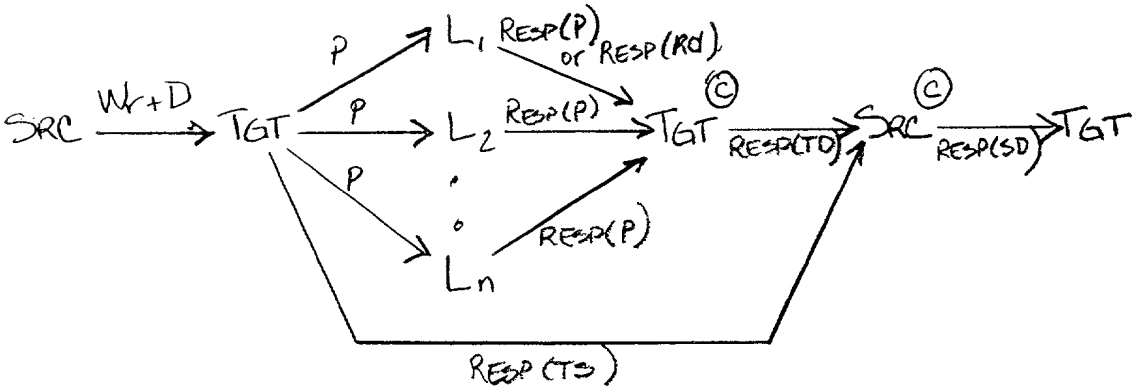
SRC
Wr+D
TGT
P
P
P
L1
L2
Ln
RESP(P) or RESP(Rd)
RESP(P)
RESP(P)
©
TGT
RESP(TD)
SRC
©
RESP(SD)
TGT
RESP (TS)

FIG. 18

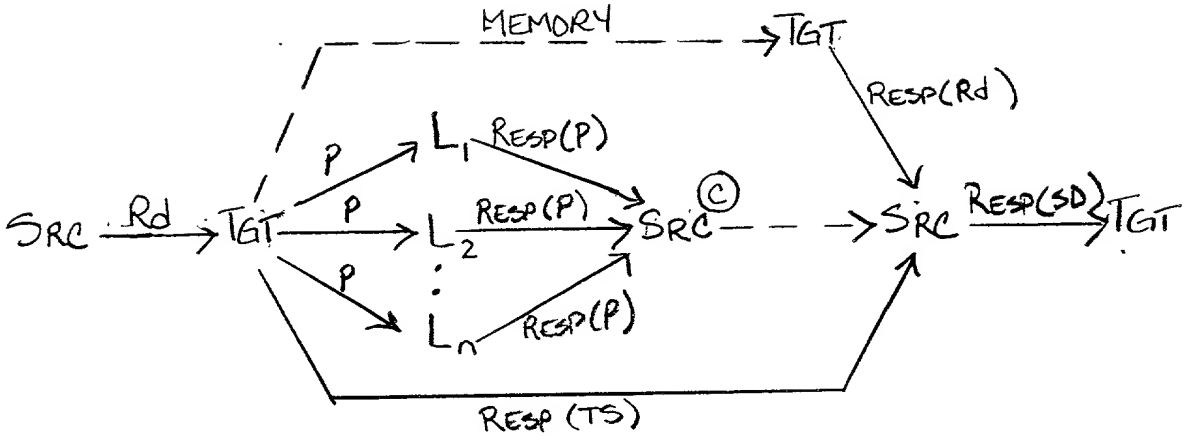
MEMORY
TGT
RESP(Rd)
P
L1
RESP(P)
SRC
Rd
TGT
P
L2
RESP(P)
SRC
SRC
RESP(SD)
TGT
P
Ln
RESP(P)
RESP (TS)

FIG. 19

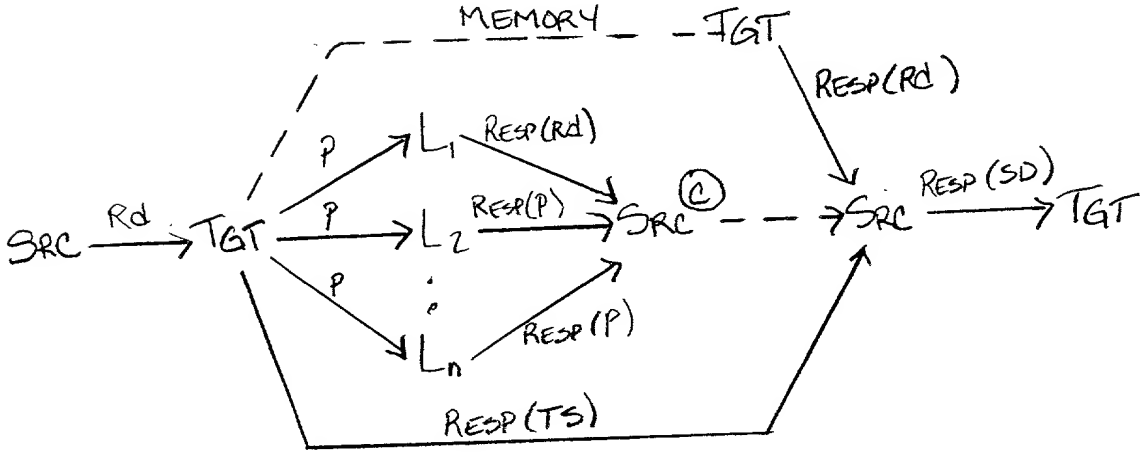
MEMORY
TGT
RESP(Rd)
P
L1
RESP(Rd)
SRC
Rd
TGT
P
L2
RESP(P)
SRC
SRC
RESP (SD)
TGT
P
Ln
RESP(P)
RESP (TS)

FIG. 20

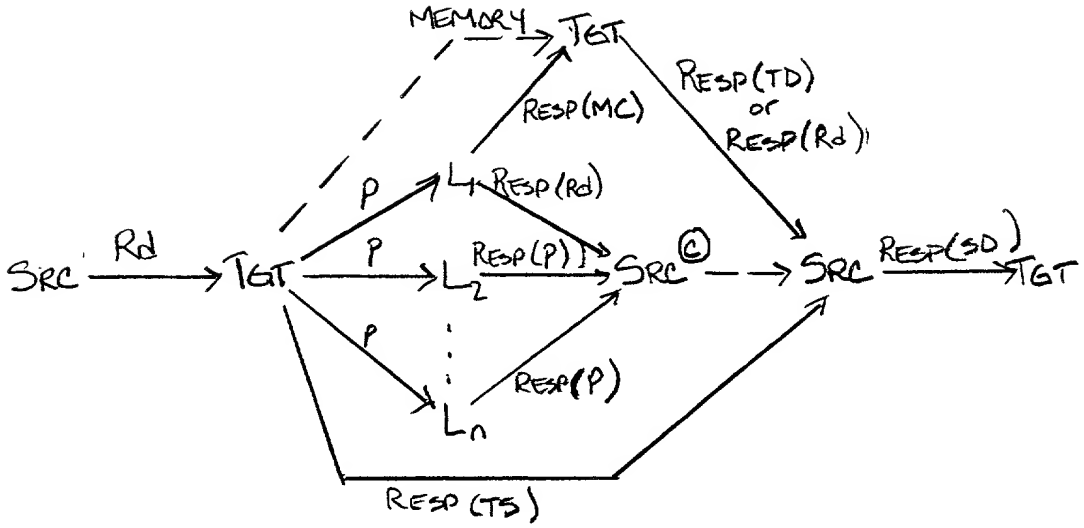
MEMORY
TGT
RESP(TD)
or
RESP(Rd)
RESP(MC)
P
L1
RESP(Rd)
SRC
Rd
TGT
P
L2
RESP(P)
SRC©
SRC
RESP(SD)
TGT
P
Ln
RESP(P)
RESP(TS)

FIG. 21

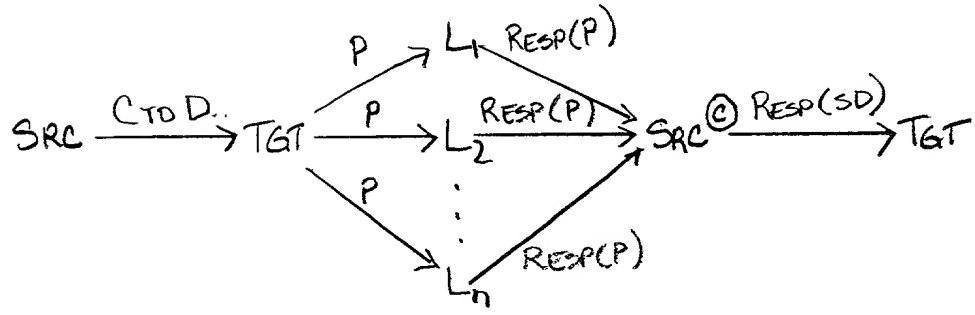
P
L1
RESP(P)
SRC
CTO D..
TGT
P
L2
RESP(P)
SRC©
RESP(SD)
TGT
P
Ln
RESP(P)

FIG. 22

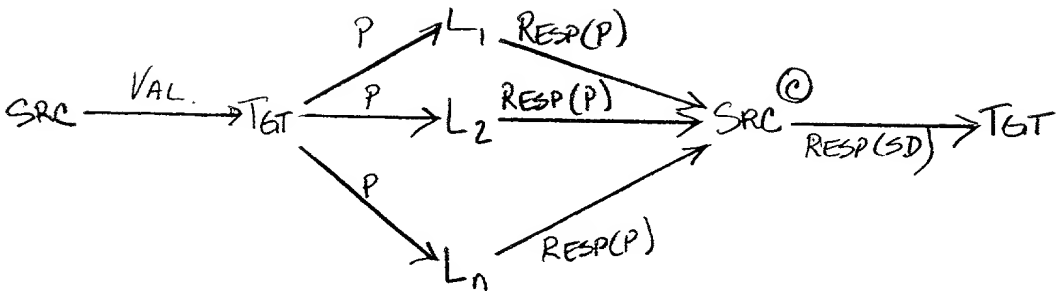

FIG. 24

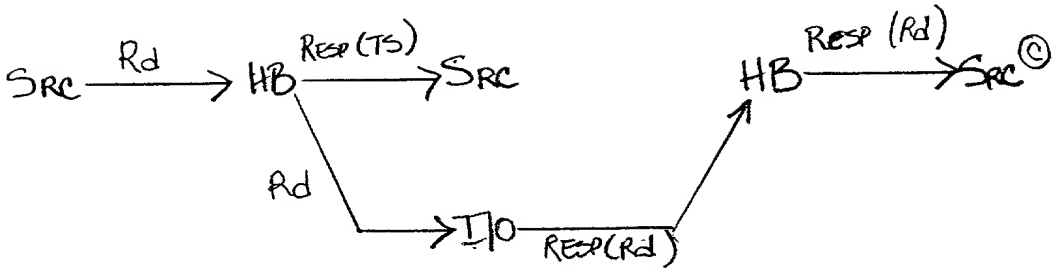

FIG. 25

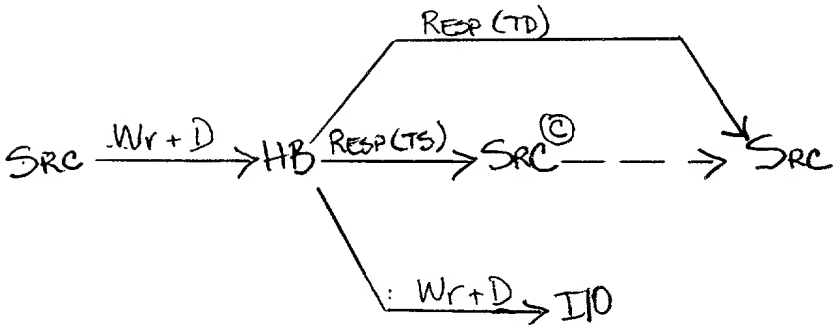

FIG. 26

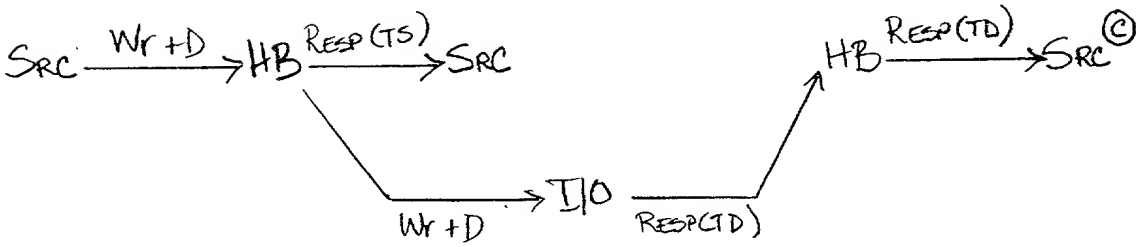

FIG. 27

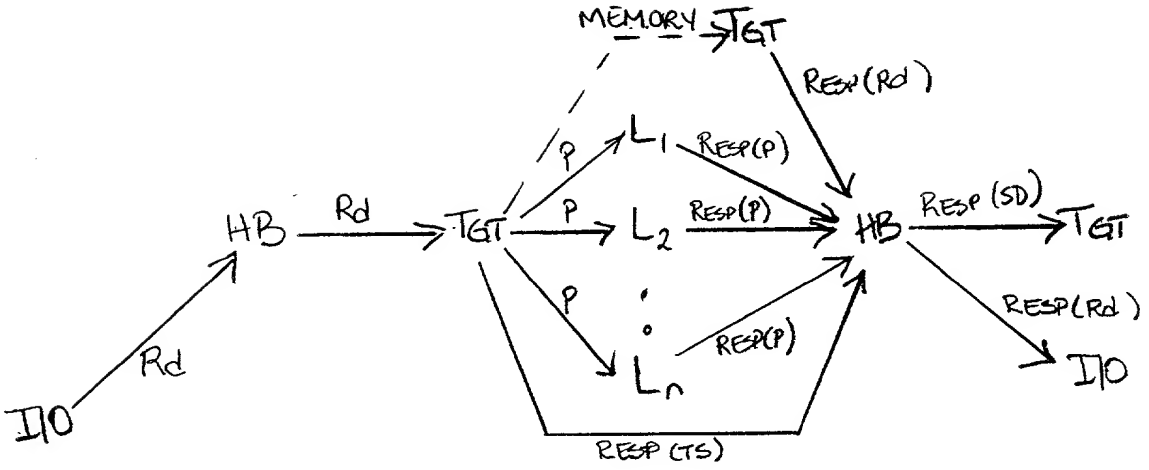
MEMORY TGT
RESP(Rd)
P
L1
RESP(P)
HB
Rd
TGT
P
L2
RESP(P)
HB
RESP (SD)
TGT
P
RESP(Rd)
Rd
Ln
RESP(P)
I/O
I/O
RESP (TS)

FIG. 28

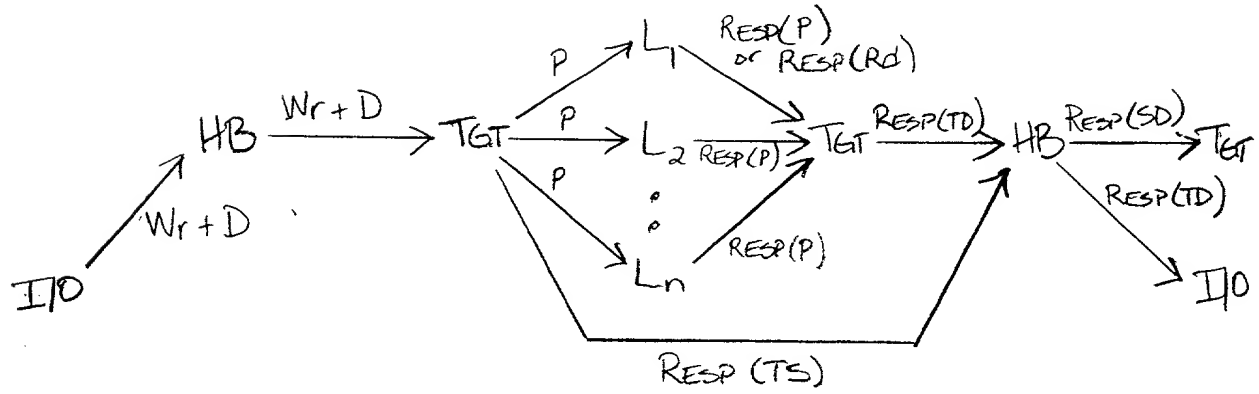
P
L1
RESP(P)
or RESP(Rd)
HB
Wr + D
TGT
P
L2
RESP(P)
TGT
RESP(TD)
HB
RESP(SD)
TGT
P
RESP(TD)
Wr + D
Ln
RESP(P)
I/O
I/O
RESP (TS)

FIG. 29

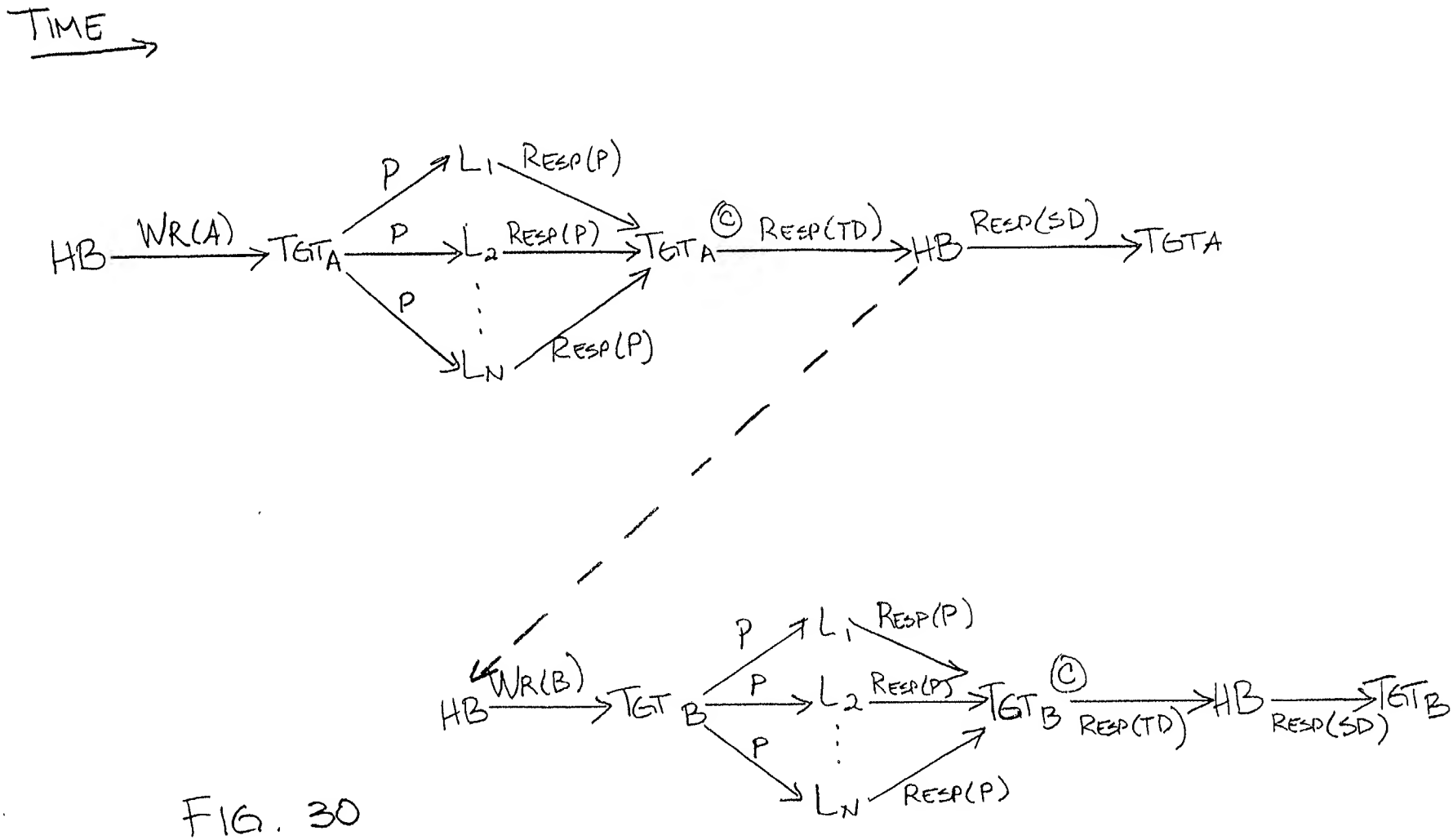

FIG. 30

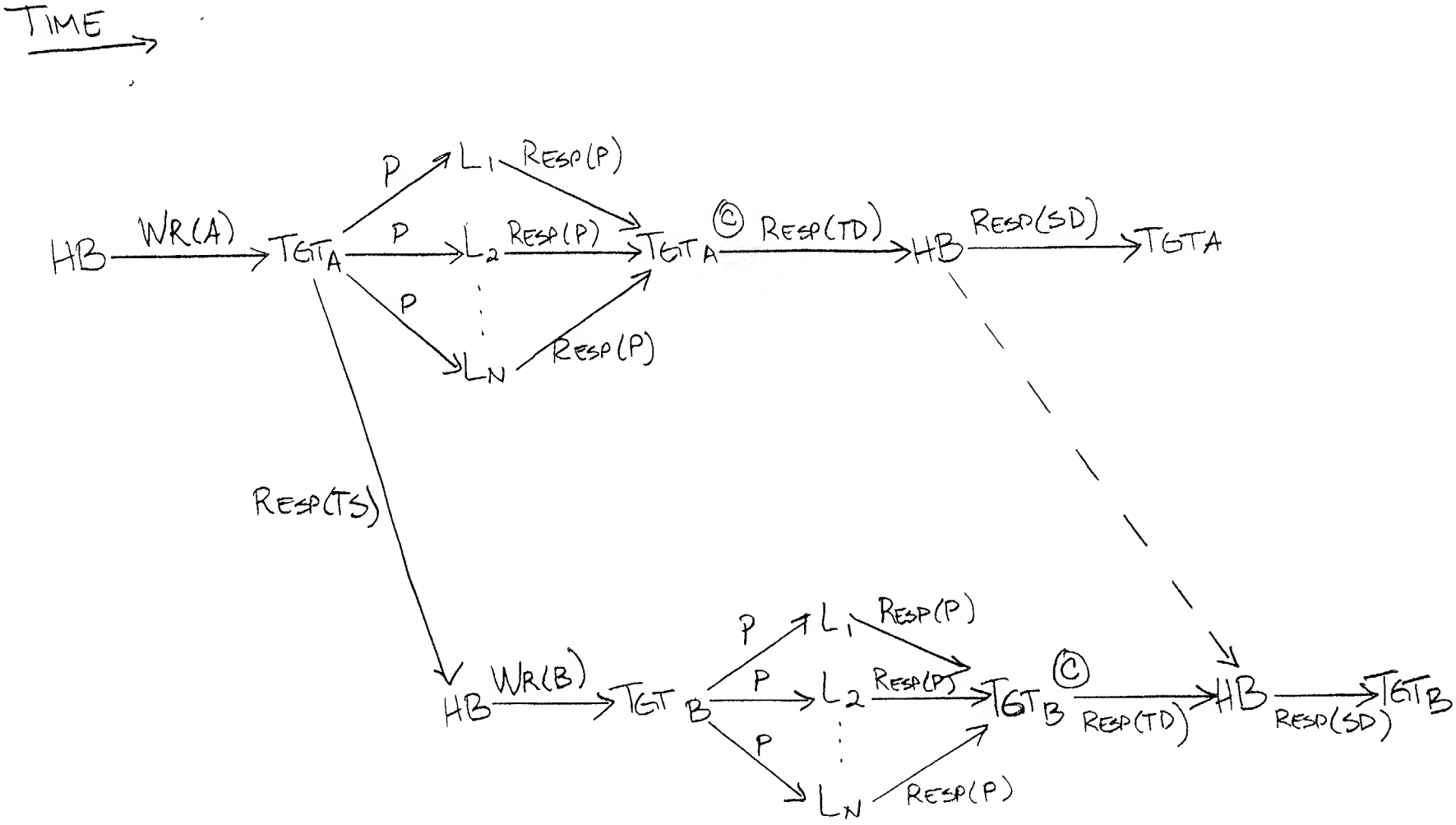

FIG. 31

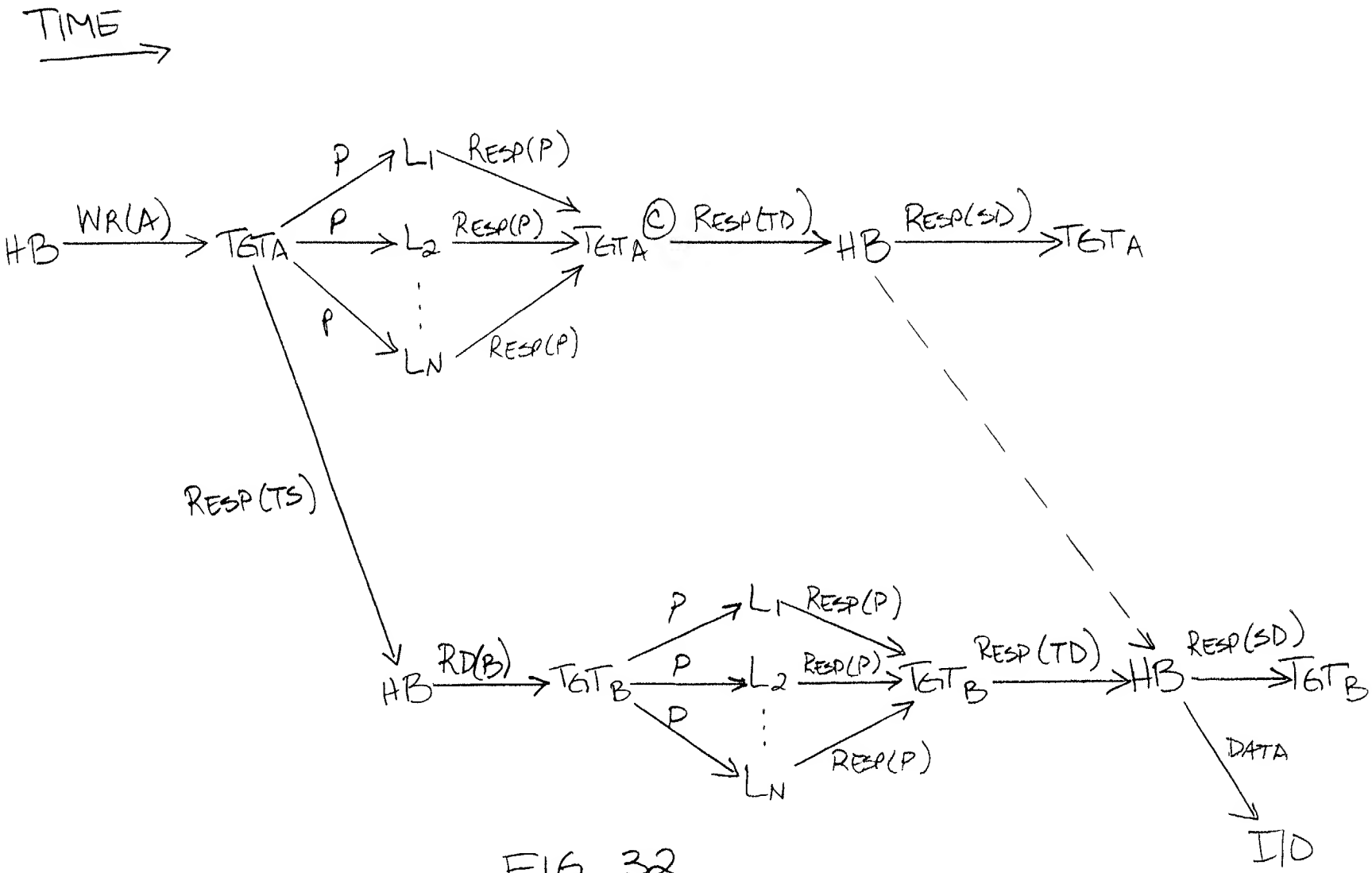

FIG. 32